1. A method of forming a capacitor device on a semiconductor substrate, comprising the steps of:

forming a shallow trench shape comprised with tapered sides, in a hard mask layer and in said semiconductor substrate;

filling said shallow trench shape with a first insulator layer resulting in a shallow trench isolation (STI) region;

removing a top portion of said first insulator layer from a first section of said STI region exposing a bare top portion of the tapered side of said first section of said STI region;

forming a second insulator layer on said bare top portion of said tapered side of said first section of said STI region;

performing an ion implantation procedure to form a capacitor region in a first portion of said semiconductor substrate located underlying said second insulator layer, and in a second portion of said semiconductor substrate located adjacent to said first portion of said semiconductor substrate, underlying a hard mask layer;

removing said hard mask layer and said second insulator layer;

forming a third insulator layer on said bare top portion of said tapered side in said first section of said STI region, and on top surface of said semiconductor substrate; and

forming a conductive structure on a second section of said STI region, on recessed, said first section of said STI region, and on said third insulator layer.

2. The method of claim 1, wherein said tapered sides of said shallow trench shape are comprised at an angle between about 70 to 89 ° in relation to a horizontal top surface of said semiconductor substrate.

3. The method of claim 1, wherein said first insulator layer is a silicon oxide layer, deposited to a thickness between about 4000 to 8000 Angstroms via a high density plasma (HDP) deposition procedure.

4. The method of claim 1, wherein the thickness of said first insulator removed from said top portion of said first section of said STI region is between about 1000 to 3500 Angstroms.

5. The method of claim 1, wherein said second insulator layer is a silicon oxide layer obtained at a thickness between about 50 to 300 Angstroms via thermal oxidation procedures.

6. The method of claim 1, wherein said ion implantation procedure, used to form said capacitor region, is performed using boron or BF_2 ions, at an energy between about 3 to 30 KeV, and at a dose between about 1E13 to 5E15 atoms/cm^2.

7. The method of claim 1, wherein said third insulator layer is a silicon dioxide layer obtained at a thickness between about 10 to 100 Angstroms, via thermal oxidation procedures.

8. The method of claim 1, wherein said conductive structure, formed on said second section of said STI region, on recessed, first section of said STI region, and on said third insulator layer, is comprised of polysilicon.

9. A method of forming a capacitor device on a semiconductor substrate, comprising the steps of:

forming a hard mask layer on said semiconductor substrate, comprised of a silicon nitride layer on an underlying silicon oxide layer;

forming a shallow trench shape comprised with tapered sides in said hard mask layer and in said semiconductor substrate;

forming a liner layer on all surfaces of said shallow trench shape;

depositing a silicon oxide layer completely filling said shallow trench shape, resulting in a shallow trench isolation (STI) region;

performing a capacitor patterning procedure removing a top portion of said silicon oxide layer located in a first section of said STI region and removing a top portion of said liner layer, exposing a bare top portion of the tapered side in a recessed, said first section of said STI region;

forming a screen oxide layer on said bare top portion of said tapered side in the recessed, said first section of said STI region;

performing an ion implantation procedure to form a capacitor region in a first portion of said semiconductor substrate located underlying said screen oxide layer, and in a second portion of said semiconductor substrate located adjacent to said first portion of said semiconductor substrate, underlying said hard mask layer;

performing a planarization procedure resulting in a smooth top surface comprised of top surfaces of said STI region and of said hard mask layer;

removing said hard mask layer and said screen oxide layer;

forming a capacitor dielectric layer on said bare top portion of said tapered side in said first section of said STI region, and on top surface of said semiconductor substrate; and

forming a conductive structure on a second section of said STI region, on the recessed, said first section of said STI region, and on said capacitor dielectric layer.

10. The method of claim 9, wherein said tapered sides of said shallow trench shape are comprised at an angle between about 70 to 89 ° in relation to a horizontal top surface of said semiconductor substrate.

11. The method of claim 9, said liner layer is a silicon oxide layer obtained at a thickness between about 50 to 300 Angstroms via thermal oxidation procedures.

12. The method of claim 9, wherein said silicon oxide layer, used to fill said shallow trench shape, is deposited to a thickness between about 4000 to 8000 Angstroms via a high density plasma (HDP) deposition procedure.

13. The method of claim 9, wherein said capacitor patterning procedure is accomplished via photolithographic and reactive ion etching (RIE) procedures, using CHF_3 as an etchant for said silicon oxide layer and for said liner layer.

14. The method of claim 9, wherein the depth of recess in said first section of said STI region is between about 1000 to 3500 Angstroms.

15. The method of claim 9, wherein said screen oxide layer is a silicon oxide layer, obtained at a thickness between about 50 to 300 Angstroms via thermal oxidation procedures.

16. The method of claim 9, wherein said ion implantation procedure used to form said capacitor region, is performed using boron or BF_2 ions at an energy between about 3 to 30 KeV, and at a dose between about 1E13 to 5E15 atoms/cm^2.

17. The method of claim 9, wherein said capacitor dielectric layer is a silicon dioxide layer obtained at a thickness between about 10 to 100 Angstroms, via thermal oxidation procedures.

18. The method of claim 9, wherein said conductive structure formed on said second section of said STI region, on recessed, first section of said STI region, and on said third insulator layer, is a doped polysilicon structure.

19. A capacitor device, comprising:

an insulator filled shallow trench isolation (STI) region comprised with tapered sides, on a semiconductor substrate, wherein a first section of said STI region features a top surface located at a higher level than the top surface of said semiconductor substrate, and wherein a second section of said STI region features a top surface recessed below the top surface of said semiconductor substrate exposing an adjacent portion of said semiconductor substrate, wherein said adjacent portion of said semiconductor substrate features a smooth top surface and a tapered side;

an insulator layer lining all surfaces of said insulator filled STI region;

a capacitor dielectric layer on said smooth top surface, and on said tapered side of said portion of semiconductor substrate located adjacent to recessed, said second STI section;

a capacitor region in said semiconductor substrate located underlying said capacitor dielectric layer;

a conductive structure comprised with a first portion located on said capacitor dielectric layer, and with a second portion located on a portion of said first section of said insulator filled STI region; and

a metal silicide layer located on a top surface of said conductive structure.

20. The capacitor device of claim 19, wherein said tapered sides of said insulator filled STI region are at an angle between about 70 to 89 ° in relation to a horizontal top surface of said semiconductor substrate.

21. The capacitor device of claim 19, wherein said insulator layer, lining the surfaces of said insulator filled STI region, is a silicon oxide layer at a thickness between about 50 to 300 Angstroms.

22. The capacitor device of claim 19, wherein the depth of recess in said second section of said insulator filled STI region, below the top surface of said first section of said insulator filled STI region, is between about 1000 to 3500 Angstroms.

23. The capacitor device of claim 19, wherein the insulator in said insulator filled STI region is silicon oxide.

24. The capacitor device of claim 19, wherein said capacitor region is located either in an N type or P type region.

25. The capacitor device of claim 19, wherein said capacitor dielectric layer is a silicon dioxide layer, at a thickness between about 10 to 100 Angstroms.

26. The capacitor device of claim 19, wherein said conductive structure is a doped polysilicon structure.

27. The capacitor device of claim 19, wherein said metal silicide layer is comprised of either titanium silicide, tantalum silicide, cobalt silicide, nickel silicide or zirconium silicide.